REMARKS

In response to the pending Office Action, claims 4, 5, and 12 have been amended. Claims 25-38 have been added. Claim 24 has been cancelled without disclaimer of subject matter and/or prejudice. Support for the amendments may be found, for example, at page 13, lines 2-14; page 14, lines 18-25; and Figs. 2 and 4 of the present application. Support for the new claims may be found, for example, at page 4, lines 3-11; page 11, lines 1-18; page 13, line 2 to page 14 line 2; page 15, lines 9-17; page 16, lines 3-15; page 28, lines 17-21; and Figs. 2 and 4 of the present application. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Claim Rejections - 35 U.S.C. §102

Claims 4, 12, 14, and 16 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Number 4,553,159 ("Moraillon"). Claims 5, 15, 18, 19, 21, 23, and 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 6,124,888 ("Terada"). Applicants respectfully traverse these rejections for at least the following reasons.

A. Independent Claims 4 and 12 are allowable over Moraillon

As amended, claim 4 recite a solid state imaging apparatus that includes, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a first shift register for sequentially outputting selection signals, which drive each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction, and a second shift register for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a

horizontal direction. Each of the selection signals of the first shift register and each of the selection signals of the second shift register are output to a corresponding pixel included in a pixel group arranged in the same direction as the first and second shift registers, such that all pixels in the pixel group receive a selection signal from the first shift register and the second shift register.

To provide context, in one aspect, the solid state imaging apparatus according to the instant application and a camera using such solid state imaging apparatus, can make it possible to switch between a regular operation and a mixing operation. In the regular operation, selection signals driving each signal are output sequentially to all pixels arranged in a row or a column, and in the mixing operation, the selection signals are continuously output to some of the pixels arranged in a row or a column and having color filters of a same color. Moreover, each of the selection signals of the first shift register and each of the selection signals of the second shift register are output to a corresponding pixel included in a pixel group arranged in the same direction as the first and second shift registers, such that all pixels in the pixel group receive a selection signal from the first shift register and the second shift register.

Accordingly, such solid state imaging apparatus and such camera can prevent the occurrence of a false color due to omission of pixel information when image pickup is performed to a moving image in a mixing operation as well as to a static image in a regular operation.

Moraillon, in FIG. 3, discloses a color television camera including a photosensitive matrix, an output circuit, and a pixel selection circuit. The output circuit includes a first horizontal shift register (12) and a second horizontal shift register (13), respectively arranged above and below the photosensitive matrix. The pixel selection circuit includes a first vertical

shift register (14) and a second vertical shift register (15), respectively arranged to the right and left sides of the photosensitive matrix.

The first horizontal shift register (12) outputs signals G aligned in the vertical direction, while the second horizontal shift register (13) outputs signals R and signals B of even lines. However, each signal of the first horizontal shift register (12) and each signal of the second horizontal shift register (13) are merely output from a half of pixels included in a pixel group arranged in the horizontal direction, not from all of the pixels. Also, each selection signal of the first vertical shift register (14) and each selection signal of the second vertical shift register (15) is not output to all pixels included in a pixel group arranged in the vertical direction.

In contrast, as shown in Fig. 2, in the instant application each of the selection signals of the first shift register (e.g., register (11)) and each of the selection signals of the second shift register (e.g., register (12)) are output to a corresponding pixel included in a single line pixel group 10, such that all pixels in the pixel group receive a selection signal from the first shift register and the second shift register.

As such, Moraillon fails to describe or suggest a solid state imaging apparatus that includes, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a first shift register for sequentially outputting selection signals, which drive each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction, and a second shift register for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction, wherein each of the selection signals of the first shift register and each of the selection signals of the second shift register are output to a corresponding pixel included in a pixel group arranged in the same direction as the first and second shift registers,

*such that **all** pixels in the pixel group receive a selection signal from the first shift register and the second shift register*, as recited in claim 4.

Furthermore, in Moraillon, the first and second horizontal shift registers (12, 13) are charge coupling registers (CCD's), i.e. charge transfer lines for receiving signals from each pixel and outputting the signals to an external apparatus. In contrast, in the instant application, as shown in Fig. 2, each of the selection signals of the first shift register (e.g., register (11)), which are arranged in the vertical direction, and each of the selection signals of the second shift register (e.g., register (12)) are output to pixels included in a single line pixel group 10 arranged in the vertical direction. That is, in one aspect, the first and second shift registers of the instant application are drive circuits of pixels outputting selection signals (scan pulses) which drive each pixel to a pixel group.

Accordingly, the alleged first shift register (e.g., the first horizontal shift register (12)) does not correspond to a first shift register for sequentially ***outputting*** selection signals, which ***drive*** each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction, as recited in claim 4. Similarly, the alleged second shift register (e.g., the second horizontal shift register (13)) does not correspond to a second shift register for continuously ***outputting*** the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction, as recited in claim 4.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 4. Claim 12 has been amended to recite features similar to the above-recited features of claim 4. Therefore, for at least the reasons presented above with respect to claim 4, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 12.

B. Independent Claim 5 is allowable over Terada

As amended, claim 5 recites a solid state imaging apparatus that includes, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a shift register for sequentially outputting selection signals, which drive each pixel, to all of the plurality of pixels either in a vertical or a horizontal direction, and an operation switching circuit for outputting the selection signals from the shift register to each pixel, the operation switching circuit configured to switch between a first signal transmission method in which the selection signals are sequentially output to some pixels either in the vertical direction or the horizontal direction and a second signal transmission method in which the selection signals are continuously output to all pixels having color filters of the same color either in the vertical direction or the horizontal direction. In both of the first and second signal transmission methods, each of the selection signals of the shift register is output via the operation switching circuit to a corresponding pixel included in a pixel group arranged in the same direction as the shift register, such that all pixels in the pixel group receive a selection signal from the shift register.

Accordingly, the solid state imaging apparatus of the claimed subject matter can prevent the occurrence of a false color due to omission of pixel information when image pickup is performed to a moving image in a mixing operation as well as to a static image in a regular operation.

Terada, in Fig. 26, discloses an imaging apparatus in which signals of four shadowed pixels are added and read out, when line 1 and line 3 are selected by a vertical shift register (609), and row 4 and row 6 are selected by switching between SWs driven by a horizontal shift register (610). However, in Terada, each signal of the horizontal shift register (610) is not

output to all the switches arranged in the horizontal direction, or to the output signal line (611) from all pixels included in a single line pixel group arranged in the horizontal direction and connected to each switch.

Furthermore, in Terada, as shown in Figs. 27A and 27B, omission of pixel signals may occur when image pick-up is performed in a moving image mode. For example, a signal G of the primary unit of (X, Y)=(1, 1) in Fig. 27B outputs the addition of four signals G of (X, Y)=(1, 1), (3, 1), (1, 3) and (3, 3), but not the four signals, (X, Y)=(2, 2), (4, 2), (2, 4) and (4, 4). That is, in Terada, some pixel signals are thinned in a moving image mode and not all of the pixel signals are used (see, col. 26, lines 44-62 of Terada).

In contrast, in one aspect of the instant application as shown in Fig. 4, in the second signal transmission method (corresponding to a moving image mode) as well as the first signal transmission method, each selection signal of the vertical shift register (21) is output via an operation switching circuit to a corresponding pixel included in a single line pixel group (20) arranged in a vertical direction, such that all pixels in the pixel group (20) receive a selection signal from the shift register (21). That is, even when image pick-up is performed in a moving picture mode, all pixel signals are output without being thinned.

As such, Terada fails to describe or otherwise suggest a solid state imaging apparatus that includes, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a shift register for sequentially outputting selection signals, which drive each pixel, to all of the plurality of pixels either in a vertical or a horizontal direction, and an operation switching circuit for outputting the selection signals from the shift register to each pixel, the operation switching circuit configured to switch between a first signal transmission method in which the selection signals are sequentially output to some

pixels either in the vertical direction or the horizontal direction and a second signal transmission method in which the selection signals are continuously output to all pixels having color filters of the same color either in the vertical direction or the horizontal direction, wherein in both of the first and second signal transmission methods, each of the selection signals of the shift register is output via the operation switching circuit to a corresponding pixel included in a pixel group arranged in the same direction as the shift register, *such that **all** pixels in the pixel group receive a selection signal from the shift register*, as recited in claim 5.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 5.

New Claims

Independent claim 31 recites, among other features, a first shift register of the pair of shift registers outputting the selection signals in number order, and a second shift register of the pair of shift registers outputting the selection signals, changing the order partially. Independent claim 35 recites, among other features, in a first signal transmission method of the two signal transmission methods, the shift register outputs the selection signals in number order, and in a second signal transmission method of the two signal transmission methods, the shift register outputs the selection signals, changing the order partially.

It is noted that none of the cited references or any combination thereof appear to disclose or suggest the structure corresponding to the second shift register or second signal transmission method respectively recited in claims 31 and 35, in which the shift register outputs selection signals, changing the order partially. Therefore, it is submitted that claims 31 and 35 are patentable over the cited references.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 4, 5, 12, 31, and 35 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are allowable over the cited prior art. Accordingly, it is respectfully requested that the rejection under § 102/103 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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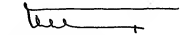

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